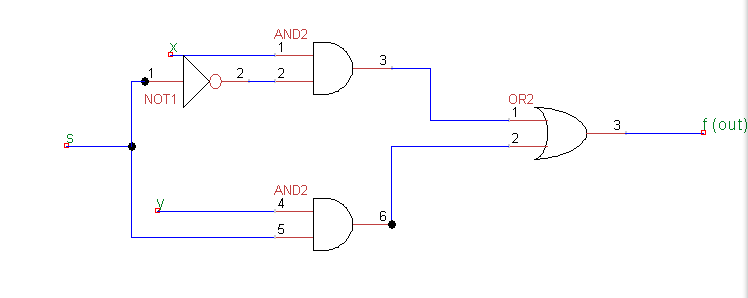
**Lab1 Pre-lab Report**

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**Part 1**

1. Draw a circuit design for f = xs’ + ys

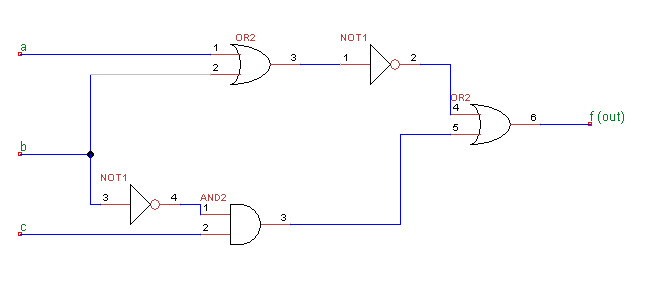


1. Write out the truth table for above design

|  |  |  |  |
| --- | --- | --- | --- |
| x | y | s | f |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Part 2**

1. Draw a circuit design for f = (a + b)’ + cb’



1. Write out the truth table for above design.

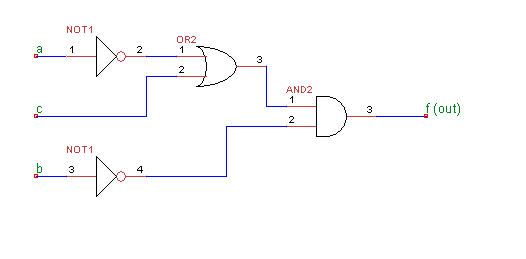
|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | f |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

4. Rewrite a cheaper implementation for above design.

f = (a + b)’ + cb’

= a’b’ + cb’

= b’(a’ + c)



By using this implementation, we get the same truth table and this implementation uses one OR gate less.